The invention claimed is:

1. A manufacturing method for a semiconductor device comprising:

forming layers of gate dielectric material, gate material, and cap material on a semiconductor substrate;

processing the cap material and a portion of the gate material to form a cap and a gate body portion;

forming a wing on the gate body portion from a remaining portion of the gate material;

removing the gate dielectric material under a portion of the wing on the gate body portion to form a gate dielectric; and

forming a lightly-doped source/drain region in the semiconductor substrate using the gate body portion and the wing.

2. The method as claimed in claim 1 wherein forming the wing includes rounding the outside edge thereof.

3. The method as claimed in claim 1 further comprising:

forming a first spacer around the gate body portion and over the remaining portion of the gate material and the gate dielectric material; and

forming the lightly-doped source/drain region additionally using the first spacer.

4. The method as claimed in claim 1 further comprising:

forming a first spacer around the gate body portion and over the remaining portion of the gate material and gate dielectric material;

forming a second spacer around the first spacer;

removing the remaining portion of the gate material except under the first spacer, the second spacer, and the cap; and

removing the gate dielectric material under the portion of the wing removes the gate dielectric material under the second spacer.

5. The method as claimed in claim 4 further comprising:

forming a third spacer around the gate body portion and the gate dielectric; and

removing the first spacer and the second spacer.

6. The method as claimed in claim 4 further comprising:

removing the first spacer and the second spacer;

forming a further spacer around the gate body portion and the gate dielectric; and

forming a source/drain region in the semiconductor substrate using the further spacer.

7. The method as claimed in claim 1 further comprising forming a metal contact over the gate body portion.

8. A manufacturing method for a semiconductor device comprising:

forming layers of silicon dioxide or nitrided oxide material, amorphous or polycrystalline silicon, and nitride cap material on a silicon substrate;

processing the nitride cap material and a portion of the amorphous or polycrystalline silicon to form a nitride cap and an amorphous or polycrystalline silicon gate body portion;

forming an amorphous or polycrystalline silicon wing on the amorphous or polycrystalline silicon gate body portion from a remaining portion of the amorphous or polycrystalline silicon to form an amorphous or polycrystalline silicon wing gate;

removing the silicon dioxide or nitrided oxide material under a portion of the amorphous or polycrystalline silicon gate wing to form a gate dielectric;

forming a lightly-doped source/drain region in the semiconductor substrate using the amorphous or polycrystalline silicon wing gate; and

forming a poly metal dielectric layer over the amorphous or polycrystalline silicon wing gate.

9. The method as claimed in claim 8 wherein forming the amorphous or polycrystalline silicon gate wing includes rounding the outside edge thereof using a high temperature/high pressure oxidation.

10. The method as claimed in claim 8 further comprising:

forming a nitride first spacer around the amorphous or polycrystalline silicon gate body portion and over the remaining portion of the amorphous or polycrystalline silicon and the silicon dioxide or nitrided oxide material; and

forming the lightly-doped source/drain region additionally using the nitride first spacer.

11. The method as claimed in claim 8 further comprising:

forming a nitride first spacer around the amorphous or polycrystalline silicon gate body portion and over the amorphous or polycrystalline silicon and silicon dioxide or nitrided oxide material;

forming an oxide second spacer around the nitride first spacer;

removing the remaining portion of the amorphous or polycrystalline silicon except under the nitride first spacer, the oxide second spacer, and the nitride cap; and

removing the silicon dioxide or nitrided oxide material removes the silicon dioxide or nitrided oxide material under the oxide second spacer to form a gate dielectric.

12. The method as claimed in claim 11 further comprising:

removing the nitride first spacer and the oxide second spacer; and

further processing of the amorphous or polycrystalline silicon gate including an amorphous or polycrystalline re-oxidation process.

13. The method as claimed in claim 11 further comprising:

removing the nitride first spacer and the oxide second spacer;

forming an oxide further spacer around the amorphous or polycrystalline silicon gate and the gate dielectric; and

forming a source/drain region in the semiconductor substrate using the oxide further spacer.

14. The method as claimed in claim 8 further comprising forming a metal contact over the amorphous or polycrystalline silicon gate body portion.

15. A semiconductor device comprising:

a semiconductor substrate;

a gate dielectric on the semiconductor substrate, the gate dielectric having a first width;

a wing gate on the gate dielectric, the wing gate having a body portion narrower than the first width and a gate wing wider than the first width; and

a lightly-doped source/drain region in the semiconductor substrate adjacent the gate dielectric.

16. The semiconductor device as claimed in claim 15 further comprising:

a spacer wider than the first width and positioned around the wing gate; and

a source/drain region in the semiconductor substrate adjacent the spacer and connected to the lightly-doped source/drain region.

17. The semiconductor device as claimed in claim 15 wherein:
the wing gate comprises the gate wing having a rounded tip.

18. The semiconductor device as claimed in claim 15 further comprising:
a metal contact over the wing gate.

19. A semiconductor device comprising:
a silicon substrate;
a gate dielectric on the silicon substrate, the gate dielectric having a first width;
a wing gate on the gate dielectric, the wing gate of amorphous or polycrystalline silicon having a body portion narrower than the first width and a gate wing wider than the first width; and
a lightly-doped source/drain region in the silicon substrate adjacent the gate dielectric.

20. The semiconductor device as claimed in claim 19 further comprising:
an oxide spacer wider than the first width and positioned around the wing gate; and
a source/drain region in the silicon substrate adjacent the oxide spacer and connected to the lightly-doped source/drain region.

21. The semiconductor device as claimed in claim 19 wherein:
the wing gate comprises the gate wing having a rounded tip;
a source/drain region in the silicon substrate connected to the lightly-doped source/drain region; and
an oxide spacer wider than the first width and positioned around the wing gate, the oxide spacer cooperating with the gate wing to form a three-step source/drain profile of the lightly-doped source/drain region and the source/drain region.

22. The semiconductor device as claimed in claim 19 further comprising:
a metal contact over the body portion of the wing gate.